What is claimed is:

1. A reversible logic element comprising:

three input lines {T, T', S} from which a signal can be input;

three output lines {T_A, T_B, S'} to which the signal can be output by output means;

state control means for controlling two states (an A-state and a B-state);

input information identification means for identifying which of the three input lines the signal is input from;

state determination means for determining whether the reversible logic element is in the A-state or the B-state; and

control means, wherein

if said state determination means determines that said reversible logic element is in the A-state and the signal is input from the input line T, then said state determination means conveys information that said reversible logic element is in the A-state to said control means, said input information identification means conveys information that the signal is input from the input line T to said control means, and said control means controls said output means to output the signal to the output line T_A and controls the state control means to change the state of the reversible logic element to the B-state,

if said state determinations means determines that said reversible logic element is in the B-state and the signal is input from the input line T, then said state determination means conveys information that said reversible logic element is in the B-state to said control means, said input information identification means conveys the information that the signal is input from the input line T to said control means, and said control means controls said output means to output the signal to the output line T_B and controls said state control means to change the state of the reversible logic element to the A-state,

if said state determinations means determines that said reversible logic element is in the A-state and the signal is input from the input line S, then said state determination means conveys the information that said reversible logic element is in the A-state to said control means, said input information identification means conveys information that the signal is input from the input

line S to said control means, and said control means controls said output means to output the signal to the output line S' while keeping said reversible logic element in the A-state,

if said state determinations means determines that said reversible logic element is in the B-state and the signal is input from the input line S, then said state determination means conveys the information that said reversible logic element is in the B-state to said control means, said input information identification means conveys the information that the signal is input from the input line S to said control means, and said control means controls said output means to output the signal to the output line T_A and controls said state control means to change the state of said reversible logic element to the A-state, and

if said state determinations means determines that said reversible logic element is in the B-state and the signal is input from the input line T', then said state determination means conveys the information that said reversible logic element is in the B-state to said control means, said input information identification means conveys information that the signal is input from the input line T' to said control means, and said control means controls said output means to output the signal to the output line T_B while keeping said reversible logic element in the B-state.

2. The reversible logic element according to claim 1, wherein said signal is an electric signal.

3. A method for constructing a logic circuit using the reversible logic element according to claim 1.

4. A method for constructing a computer using the reversible logic element according to claim 1.

5. A program for allowing a computer to function as the reversible logic element according to claim 1.

6. A recording medium recording the program according to claim 5.

7. A reversible logic element having three input lines {T, T', S} from which a signal can be input, three output lines {T_A, T_B, S'} to which the signal can be output by output means, two states (an A-state and a B-state) controllable by state control means, the reversible logic element comprising:

input information identification means for identifying which of the three input lines the signal is input from;

state determination means capable of determining whether the reversible logic element is in the A-state or the B-state; and

control means, wherein

if said state determination means determines that said reversible logic element is in the A-state and the signal is input from the input line T, then said state determination means conveys information that said reversible logic element is in the A-state to the control means, said input information identification means conveys information that the signal is input from the input line T to said control means, and said control means controls said output means to output the signal to the output line T_A and controls said state control means to change the state of the reversible logic element to the B-state,

if said state determinations means determines that said reversible logic element is in the B-state and the signal is input from the input line T, then said state determination means conveys information that said reversible logic element is in the B-state to said control means, said input information identification means conveys the information that the signal is input from the input line T to said control means, and said control means controls the output means to output the signal to the output line T_B and controls the state control means to change the state of the reversible logic element to the A-state,

if said state determinations means determines that said reversible logic element is in the A-state and the signal is input from the input line S, then said state determination means conveys the information that said reversible logic element is in the A-state to said control means, said input information identification means conveys information that the signal is input from the input line S to said control means, and said control means controls the output means to output the signal to the output line S' while keeping said reversible logic element in the A-state,

if said state determinations means determines that said reversible logic element is in the B-state and the signal is input from the input line S, then said state determination means conveys the information that said reversible logic element is in the B-state to said control means, said input information identification means conveys the information that the signal is input from the input line S to said control means, and said control means controls said output means to output the signal to the output line T_A and controls said state control means to change the state of said reversible logic element to the A-state,

if said state determinations means determines that said reversible logic element is in the A-state and the signal is input from the input line T', then said state determination means conveys the information that said reversible logic element is in the A-state to said control means, said input information identification means conveys information that the signal is input from the input line T' to said control means, and said control means controls said output means to output the signal to the output line S' and controls said state control means to change the state of said reversible logic element to the B-state; and

if said state determinations means determines that said reversible logic element is in the B-state and the signal is input from the input line T', then said state determination means conveys the information that said reversible logic element is in the B-state to said control means, said input information identification means conveys information that the signal is input from the input line T' to said control means, and said control means controls said output means to output the signal to the output line T_B while keeping said reversible logic element in the B-state.

8. The reversible logic element according to claim 7, wherein said signal is an electric signal.

9. A method for constructing a logic circuit using the reversible logic element according to claim 7.

10. A method for constructing a computer using the reversible logic element according to claim 7.

11. A program for allowing a computer to function as the reversible logic element according to claim 7.

12. A recording medium recording the program according to claim 11.

13. A reversible logic element group comprising: a first reversible logic element; and a second reversible logic element, wherein

the first reversible logic element has two input lines {S, T} from which a signal can be input, two output lines $\{T_A, T_B\}$ to which the signal can be output by output means, two states (an A-state and a B-state) controllable by state control means, the first reversible logic element comprising: input information identification means for identifying which of the two input lines the signal is input from; state determination means capable of determining whether the first reversible logic element is in the A-state or the B-state; and control means, and

if said state determination means determines that said first reversible logic element is in the A-state and the signal is input from the input line T, then said state determination means conveys information that said first reversible logic element is in the A-state to said control means, said input information identification means conveys information that the signal is input from the input line T to said control means, and said control means controls the output means to output the signal to said output line T_A and controls said state control means to change the state of said first reversible logic element to the B-state,

if said state determinations means determines that said first reversible logic element is in the B-state and the signal is input from the input line T, then said state determination means conveys information that said first reversible logic element is in the B-state to said control means, said input information identification means conveys the information that the signal is input from the input line T to said control means, and said control means controls said output means to output the signal to the output line T_B and controls said state control means to change the state of said first reversible logic element to the A-state,

if said state determinations means determines that said first reversible logic element is in the A-state and the signal is input from the input line S, then said state determination means conveys the information that said first reversible logic element is in the A-state to said control means, said input information identification means conveys information that the signal is input from the input line S to said control means, and said control means controls said output means to output the signal to the output line T_A and controls said state control means to keep the state of said first reversible element in the A-state, and

if said state determinations means determines that said first reversible logic element is in the B-state and the signal is input from the input line S, then said state determination means conveys the information that said first reversible logic element is in the B-state to said control means, said input information identification means conveys the information that the signal is input from the input line S to said control means, and said control means controls said output means to output the signal to the output line T_B and controls said state control means to keep said first reversible logic element in the B-state; and wherein

a second reversible logic element has two input lines $\{T_A, T_B\}$ from which a signal can be input, two output lines {S, T} to which the signal can be output by output means, two states (an

A-state and a B-state) controllable by state control means, the second reversible logic element comprising: input information identification means for identifying which of the two input lines the signal is input from; state determination means capable of determining whether the second reversible logic element is in the A-state or the B-state; and control means, wherein

if said state determination means determines that said second reversible logic element is in the B-state and the signal is input from the input line T_A, then said state determination means conveys information that said second reversible logic element is in the B-state to the control means, said input information identification means conveys information that the signal is input from the input line T_A to said control means, and said control means controls said output means to output the signal to the output line T and controls said state control means to change the state of said second reversible logic element to the A-state,

if said state determinations means determines that said second reversible logic element is in the A-state and the signal is input from the input line T_B, then said state determination means conveys information that said second reversible logic element is in the A-state to said control means, said input information identification means conveys information that the signal is input from the input line T_B to said control means, and said control means controls said output means to output the signal to the output line T and controls said state control means to change the state of said second reversible logic element to the B-state,

if said state determinations means determines that said second reversible logic element is in the A-state and the signal is input from the input line T_A, then said state determination means conveys the information that said second reversible logic element is in the A-state to said control means, said input information identification means conveys the information that the signal is input from the input line T_A to said control means, and said control means controls the output means to output the signal to the output line S and controls said state control means to keep the state of said second reversible element in the A-state, and

if said state determinations means determines that said second reversible logic element is in the B-state and the signal is input from the input line T_B, then said state determination means conveys the information that said second reversible logic element is in the B-state to said control means, said input information identification means conveys the information that the signal is input from the input line T_B to said control means, and said control means controls said output

means to output the signal to the output line S and controls said state control means to keep said second reversible logic element in the B-state.

14. The reversible logic element group according to claim 13, wherein said signal is an electric signal.

15. A method for constructing a logic circuit using the reversible logic element group according to claim 13.

16. A method for constructing a computer using the reversible logic element group according to claim 13.

17. A program for allowing a computer to function as the first reversible logic element and the second reversible logic element according to claim 13.

18. A recording medium recording the program according to claim 17.